Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1. (cancelled)

Claim 2. (currently amended) A system comprising:

a memory, wherein the memory includes a plurality of logical memory devices; and

a network switch coupled to the memory, the network switch including a memory controller, wherein the switch is configured to sequentially write a first portion of received packet data to a first of the plurality of logical memory devices and to write a second portion of the packet data to a second of the plurality of logical memory devices and to write a third portion of the packet data to a third of the plurality of logical memory devices and

wherein the memory controller maintains a record identifying which of the plurality of logical memory devices was last written to; and

wherein the first of the plurality of logical memory devices comprises a synchronous static random access memories (SSRAMs) and the second and third of the plurality of logical memory devices comprise synchronous dynamic random access memories (SDRAMs).

Claim 3. (canceled)

Claim 4. (previously presented) The system of claim 2 wherein the memory controller comprises:

a first memory controller component coupled to the first logical memory device; and

a second memory controller component coupled to the second logical memory device.

Claim 5. (original) The system of claim 4 wherein the first memory controller component and the second memory controller component access the corresponding logical memory devices via a shared address line.

Claims 6-8. (canceled)

Claim 9. (previously presented) The system of claim 2 wherein the network switch further comprises:

a receiver coupled to the memory controller;

a transmitter coupled to the memory controller;

address resolution logic coupled to the memory controller; and

packet queuing control coupled to the memory controller, the receiver, the transmitter and the address resolution logic.

Claim 10. (previously presented) The system of claim 9 wherein the network switch further comprises a media access controller (MAC) coupled to the receiver, wherein the MAC receives packet data via a plurality of ports coupled to the receiver.

Claims 11-19. (canceled)

Claim 20. (currently amended) A method comprising:

receiving a first data packet at a network switch;

performing a first memory write access wherein

a first portion of the first data packet is written to a first logical memory device coupled to the network switch

a second portion of the first data packet is written to a second logical memory device coupled to the network switch ~~and~~

a third portion of the first data packet is written to a third logical memory device coupled to the network switch, the third logical memory device having two banks; ~~and~~

determining at the network switch the logical memory device to which a portion of the first data packet was last written;

determining whether the size of a third portion of the data packet is less than a predetermined value; and

if so, writing the third portion of the data packet to both banks of the third logical memory device.

Claim 21. (previously presented) The method of claim 20 further comprising:

receiving a second data packet at the network switch;

writing a first portion of the second data packet to the first logical memory device; and

writing a second portion of the second data packet to the second logical memory device.

Claims 22-23. (canceled)

Claim 24. (currently amended) The method of claim 20~~23~~ further comprising:

determining whether the size of the third portion of the data packet is less than a predetermined value; and

if not, writing a first sub-portion of the third portion of the data packet to a first bank of a third logical memory device and writing a second sub-portion of the third portion of the data packet to a second bank of the third logical memory device.

Claim 25. (previously presented) A method of switching packets within a network comprising:

receiving a first data packet from a first port;

parsing the first data packet into a plurality of first data packet portions;

writing a first data packet portion of the plurality of first data packet portions to a first logical memory device of a plurality of logical memory devices;

writing a second data packet portion of the plurality of first data packet portions to a second logical memory device of the plurality of logical memory devices;

receiving a second data packet from the first port;

parsing the second data packet into a plurality of second data packet portions;

determining which of the plurality of logical memory devices was the last of the plurality of memory devices to which one of the plurality of first data packet portions was written; ~~and~~

writing a first data packet portion of the plurality of second data packet portions to the first data packet portion ~~one~~ of the plurality of logical memory devices other than the last of the plurality of memory devices;

writing the second data packet portion of the plurality of second data packet portions to a fourth logical memory device of the plurality of logical memory devices; and

writing a third data packet portion of the plurality of first data packet portions to a third logical memory device of the plurality of logical memory devices.

Claims 26-28. (canceled)

Claim 29. (previously presented) A method comprising:

receiving a first data packet at a network switch; and

performing a first memory write access wherein

a first portion of the first data packet is written to a first logical memory device coupled to the network switch

a second portion of the first data packet is written to a second logical memory device coupled to the network switch and

a third portion of the first data packet is written to a third logical memory device coupled to the network switch;

determining whether the size of a third portion of the data packet is less than a predetermined value; and if so, writing the third portion of the data packet to both banks of the third logical memory device.

Claim 30. (previously presented) The method of claim 29 further comprising:

receiving a second data packet at the network switch;

writing a first portion of the second data packet to the first logical memory device; and

writing a second portion of the second data packet to the second logical memory device.

Claim 31. (previously presented) The method of claim 30 wherein, if the size of the third portion of the data packet is not less than a predetermined value, then writing a first sub-portion of the third portion of the data packet to a first bank of a third logical memory device and writing a second sub-portion of the third portion of the data packet to a second bank of the third logical memory device.

Claim 32. (previously presented) The method of claim 29 wherein, if the size of the third portion of the data packet is not less than a predetermined value, then writing a first sub-portion of the third portion of the data packet to a first bank of a third logical memory device and writing a second sub-portion of the third portion of the data packet to a second bank of the third logical memory device.

Claim 33. (new) The method of claim 20 wherein the first, second and third logical memory devices comprise synchronous dynamic random access memories (SDRAMs).

Claim 34. (new) The method of claim 20 wherein the first logical memory devices comprises a synchronous static random access memories (SSRAMs) and the second and third logical memory devices comprise synchronous dynamic random access memories (SDRAMs).

Claim 35. (new) The method of claim 29 wherein the first, second and third logical memory devices comprise synchronous dynamic random access memories (SDRAMs).

Claim 36. (new) The method of claim 29 wherein the first logical memory devices comprises a synchronous static random access memories (SSRAMs) and the second and third logical memory devices comprise synchronous dynamic random access memories (SDRAMs).

Claim 37. (new) The system of claim 9 wherein the memory controller comprises:

a first memory controller component coupled to the first logical memory device; and

a second memory controller component coupled to the second logical memory device.

Claim 38. (new) The system of claim 35 wherein the first memory controller component and the second memory controller component access the corresponding logical memory devices via a shared address line.